ABSTRACT
Pipeline defects were known to occur in both bipolar and CMOS devices. It is reported that a possible physical correlation exists between a type of etch pit pairs (EPP) and pipeline defects on an EEPROM device. The density of EPPs, and the density of pipeline defects, was found to be significantly reduced by a 900°C anneal in nitrogen prior to N+ oxidation, and lower arsenic dose and thinner nitride in LOCOS for field isolation.

In this article, we report for the first time a strong correlation observed between pipeline defects and the presence of V/I boundary in Czochralski-grown silicon substrate on a flash memory device. In our development of a flash product, pipeline defects shorting the cell source and drain were identified to be one of the major causes of yield loss. We report for the first time a strong correlation between pipeline defects and the presence of OSF ring in wafer with V/I boundary. We found that by changing the wafer substrate type to one with no V/I boundary and optimizing the pre-LOCOS thermal cycle, we were able to eliminate the pipeline defects without negative impact on device performance.

INTRODUCTION
Pipeline defects have long been reported to cause emitter-collector shorts in bipolar devices [1]. Recently, pipeline defects have also been found in CMOS processes, causing source to drain shorts [2, 3]. Wang et al [2] suggested that the formation of pipeline defects was caused by stress generated during side wall mask isolation (SWAMI) etch at island corners. Belgal et al [3] found the correlation between pipeline defects and implant-induced damage in silicon. They eliminated the defects by introducing a low-temperature recrystallization step in an inert ambient. Soh et al [4] reported a possible physical correlation between a type of etch pit pairs (EPP) and pipeline defects on a EEPROM device. The density of EPPs, hence the density of pipeline defects, was found to be significantly reduced by a 900°C anneal in nitrogen prior to N+ oxidation, lower arsenic dose and thinner nitride in LOCOS for field isolation.

DEVICE FAILURE ANALYSIS
A 1Mb flash memory device with double diffused drain (DDD) is fabricated with P-type <100> substrate using LOCOS process.

One of the major failure mode is bitline erase failure, where all the 64 bit cells along the failed bitline are classified as failed bits under erase test. A typical bit map picture is shown in Figure 1. The total number of the failed bitlines is quite random, ranging from 1 to about 20. In our case, “Erase” is defined as high Vt state. This means if a cell is classified as failed cell after erasing, there is still large current flowing out of the bitline when read biasing condition is applied. The read condition is illustrated in Figure 2. It can be seen that the unexpectedly large current can be from the cell under read mode, or any other cells along the same bitline with gate voltage set at 0. Since all the cells on the same bitline are failed, there can be two possibilities: 1) None of the cell is erased to a Vt which is high enough to suppress large current flow when Vcg_read is applied to the gate of the selected cell; or 2) One or some of the...
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cells are very leaky even when gate bias is set to 0 so no matter which cell is being read there will always be large current flowing out of the failed bitline.

A 250 K bit cell array test structure shows that the leakage current path is from cell source to cell drain, as shown in Figure 3. This indicates a direct short between cell source and drain exists.

In addition to the electrical signature, the wafer map shows that the failed parts are distributed in a ring-like pattern near the edge of the wafer, as seen in Figure 4.

Further failure analysis revealed the existence of a pipeline defect running across several bits along the failed sub-bit line (see Figure 5). As suggested by Wang et al [2], a direct short between source and drain, possibly due to enhanced phosphorus diffusion, is believed to cause the large leakage current observed during erase test.

While very short time Wright Etch reveals the pipeline defects, longer time Wright Etch shows the existence of large amount of line shape OSF (oxidation-induced stacking fault) oriented along [110] direction. Although the OSF lines are not located exactly at the failure bits, the distribution of these stacking faults nicely overlaps the wafer map for the failed devices, i.e. ring-like distribution (see Figure 6). Further substrate analysis shows that high BMD (bulk micro-defects) density exists under the OSF ring. It is, therefore, believed that the OSF nucleate at bulk oxygen precipitates in a ring-like band pattern.

PROCESS AND SUBSTRATE MODIFICATIONS
While the formation of pipeline defects is yet to be understood, its ring-like distribution similar to OSF indicates that these two types of defects could be closely related. From our experience with previous flash processes, we have never observed any pipeline defects or ring OSF, although we used the same wafer substrates. So our approach is to eliminate the OSF ring and check whether pipeline defects are still there.

It is well known that radial position of the ring OSF depends exclusively on the growth conditions, i.e. ratio of the pull rate (v) to the interfacial axial temperature gradient at the melt/crystal interface (g) [5]. In addition, the region enclosed by the ring is known to be vacancy rich, while the

FIGURE 1

Typical MOSAID bit maps obtained after cell erase. If a single bit cell fails erase, a dark dot will be shown on the background. When all the bits along the same bit line are classified as failed bit, a dark line will be shown. In the picture at left, three failed bitlines are present.

FIGURE 2

Schematic of biasing condition during read. The large current from the failed bitline can be from any cell along the same bitline. In normal erase state, all cells including the selected cell shall be off during read and give very small amount of leakage current.

FIGURE 3

Source to drain leakage was observed for bad cell array. (The source, drain and gate of all the bits are connected in this 250k-bit cell array test structure, respectively. Only drain current is shown here for simplicity. It is confirmed that main current path is from source to drain.)

FIGURE 4

Yield wafer map shows that chips failed erase are distributed in a ring-like pattern. (Red dies failed erase)
region outside the ring is interstitial rich. In other words, the ring OSF is located close to the V/I boundary region. In fact, this is located at the so-called intermediate P-band pattern [6] of weak precipitation (the local oxide particle density in the P-band is found to be in the order of \(10^8 \text{ cm}^{-3}\)) between H- and L-bands of the heaviest precipitation.

As the existence of V/I boundary and the oxygen precipitates inside the V/I boundary are the two major criteria [7, 8], ring OSF shall not form if any one of the two criteria is not fulfilled. In order to minimize the density of oxygen precipitates, at least in the top surface of the wafer, the thermal cycle needs to be adjusted with minimum impact to device performance. In order to remove the V/I boundary from the wafer, the silicon crystal pull process is modified by adjusting the v/g ratio mentioned before. This leads to a generally vacancy-rich wafer.

A series of experiments were therefore designed to investigate the effects of various thermal conditions and process steps using various substrate types from different crystals. Wafers are pulled out at various stages to check for the existence of OSF.

Splits 1-3 are to study the effect of raising pre-LOCOS thermal process temperature. The purpose is to drive oxygen out of wafer top surface so oxygen precipitates are difficult to form in that region. For these splits, well implantation is skipped so as to focus on the effect of thermal cycle. In addition, the LOCOS process is not altered in order to minimize the impact on devices. Split 3, which employs higher temperature for pre-LOCOS processes, gives the least OSF. This result agrees with previous thought that it could be suppression of oxygen precipitation at higher temperature that tends to produce a cleaner wafer top surface with less nucleation sites for OSF to grow [6, 9]. Furthermore, the OSF density is significantly affected by the total processing time at 1150°C, as compared with the processing time at 1100°C.

In split 4 and 5, using split 3 conditions, the effect of well implantation on OSF formation is then examined. It is found that, unfortunately, the ring OSF formation is significantly enhanced with the addition of well dopants, especially phosphorus. It is not known at the moment why phosphorus can promote OSF formation, although the implant dose for both phosphorus and boron are quite similar, in the range of \(1E13\) to \(2E13\) cm\(^{-2}\). Future work can be carried out to provide an explanation.

It is very clear that with elimination of ring OSF, erase failure is also significantly reduced, therefore pipeline defects can be eliminated.
In split 6, the new wafer substrate, with adjusted v/g ratio to eliminate V/I boundary, is tested. Ring OSF is eliminated even with the addition of well implantation.

Based on the results presented above, we choose the condition stated in split 6, i.e. higher pre-LOCOS process temperature plus the new wafer substrate to check the erase failure of flash devices. The results are shown in Figure 7. It is very clear that with elimination of ring OSF, erase failure is also significantly reduced, therefore pipeline defects can be eliminated.

**DISCUSSION**

A brief summary of different flash processes that we have experienced is shown in table 2. All processes are using LOCOS scheme, but with differences in LOCOS recipe content.

It shows that pipelines may not form even with the presence of a V/I boundary. This is, we believe, related to the presence of high density OSF. Pipelines tend to form when formation of OSF is enhanced through inadequate process and wafer substrate selection. As reported elsewhere, pipeline defects have been observed to be associated with various type of dislocations, e.g. ring OSF in our case, we believe that high density of dislocations tend to promote the formation of pipeline defects. The pipeline defects can either be the same type of dislocations formed on the surface, or they can be formed through dislocations pinning at the surface region. Future work shall be directed to understand the mechanism of the pipeline defect formation and the details of the interaction between various types of dislocations with the pipeline defect formation.

**CONCLUSION**

We have established a strong correlation between the ring OSF and pipeline defects. By eliminating the V/I boundary, and optimizing the pre-LOCOS thermal cycle, we significantly reduced device failure associated with pipeline defects with minimal alteration to the device architecture. This finding further indicates that not only the IC fabrication processes but also the crystal history of the wafer substrate is critical to minimize micro-defects induced device failures such as pipeline defects.