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Cost-Effective Advanced Silicon Substrate For Next Generation IC Devices:

Improve Device Performance, Reliability, and Cost of Ownership

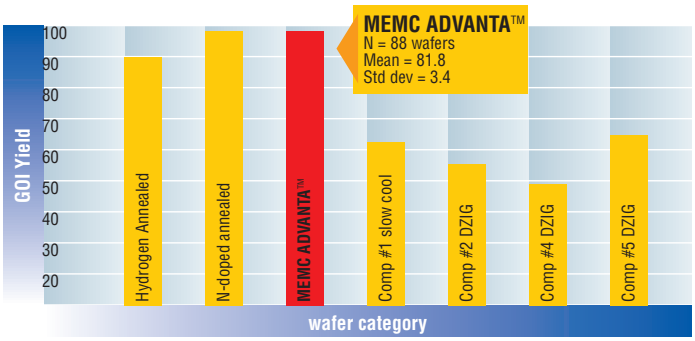
- Reduced COPs lead to higher reliability related to crystal defects
- Comparable performance with annealed wafers at much better cost
- Deep precipitate-free zone through MDZ® maintained throughout customer processing leads to improved device yield and reliability potential
- Built-in IG template through MDZ® eliminates need for customer oxygen out-diffusion and nucleation and reduces customer cycle time

The ADVANTA™ wafer

The requirements of the sub-0.25µm device generations have driven the development of several low-defect density silicon wafer alternatives. The main challenge of controlling defects in polished wafers has been to suppress the growth of agglomerated interstitial defects and vacancy defects during the crystal growth process.

ADVANTA™ polished wafers have low COPs (crystal-originated pits) and high GOI (gate oxide integrity) performance. ADVANTA's annular region outside of a central vacancy core is free of any agglomerated defects. ADVANTA™ wafers can be enhanced using MEMC's Magic Denuded Zone® (MDZ®) thermal treatment. MDZ® produces robust internal gettering protection early in the IC fabrication process.

ADVANTA™ vs. competitors wafers – GOI



(Source: MEMC AE benchmarking, 2000)

Vacancy–related defects and GOI performance

Agglomerated vacancy-related defects are known commonly as D-defects or as COPs when they intersect the wafer surface. Although recent data has shown a decreasing sensitivity of GOI to COPs at gate oxide thickness of less than 100Å, it is believed that the presence of the vacancy-related defects will have a certain impact on device performance and yield.

ADVANTA™'s COPs are reduced in number and are present only in the central core region, which produces a material with high GOI.

LPDs:
•50 max @ > 0.12 micron for 200mm
•80 max @ > 0.12 micron for 150mm

GOI:
> 65% - 85%

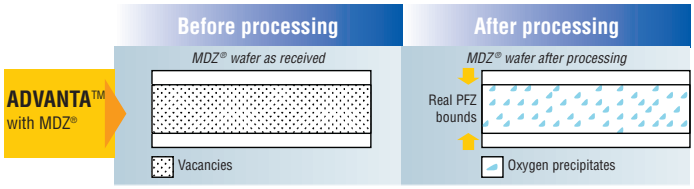
Advanced Flatness:
SFQR ≤ 0.2µm for 200mm

Intrinsic gettering

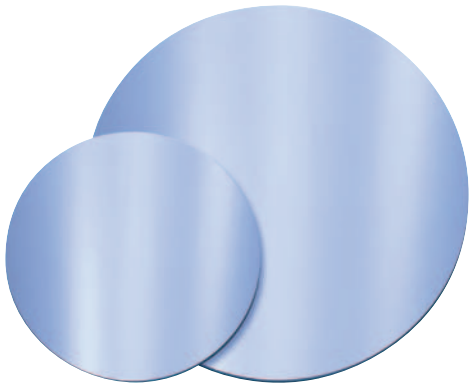
In addition to low COP densities, many customers also require intrinsic gettering. This is achieved in ADVANTA™ wafers by using MEMC's MDZ® patented process. The MDZ® process produces an ideal density of oxygen precipitates and a deep precipitate-free zone. This eliminates the need for additional, costly out-diffusion, nucleation and growth thermal cycles in the customers' manufacturing lines.

When enhanced by MDZ® ADVANTA™ offers the benefits of robust IG, reduces the risks that may lower device yields, and lowers the customer cost of ownership by IC process reduction and simplification.

The MDZ® Advantage



MDZ® installs in the ADVANTA™ wafer the right precipitate depth distribution, at the wafer level.



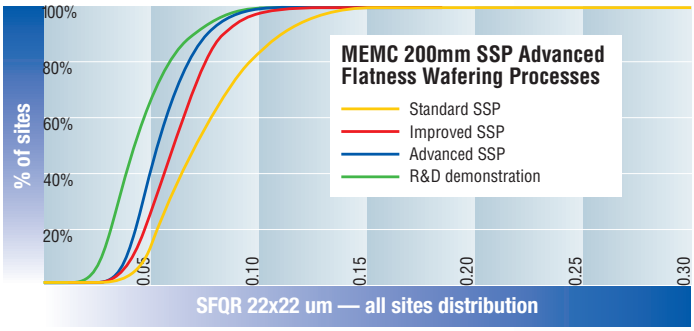
Available in 200mm and 300mm

	Standard	Slow cool	Advanta™	Annealed	Optia™	CMOS Epi (p/p+) or AEGIS™
Wafer Type	Open HZ	Vancancy-rich, no V/I boundary	Vacancy core, no V/I boundary	Low-COP, no V/I boundary	Zero COP, no V/I boundary	Zero COP, no V/I boundary
# LPDs ≥ 0.12 µm	500 max	400 max	200mm 50 max 150mm 80 max	30 max	200mm 30 max 150mm 50 max	30 max
FPD Void Density (cm^2)	300	100	200, only in core	100's (0-10 µm under surface)	0	0
GOI Yield, 200A, 10V/cm(%)	30-70	50-80	65-85	≥ 95	≥ 95	≥ 95
COP-free zone depth (µm)	0	0	Entire wafer in outer ring, 0 in core	10	Entire wafer	Epi thickness

Flatness performance

The ADVANTA™ polished wafer is manufactured by MEMC's newest wafering technology processes, which may produce flat, super-flat, and ultra-flat wafers, as required by current and next-generation IC devices.

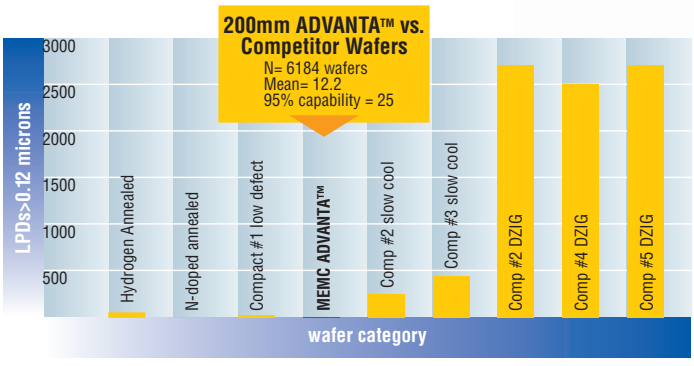
MEMC 200 mm SSP Advanced Flatness Wafering Processes



ADVANTA™ characteristics

The ADVANTA™ polished wafer is a highly reliable material for the sub-0.25µm generation IC devices, offered at great cost effectiveness compared to other advanced materials.

ADVANTA™ performance vs. competitive wafers —LPD's > 0.12 µm



(Source: MEMC AE benchmarking, 2000)

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The ADVANTA™ Advantage

- A silicon solution that will deliver yield and device performance also on advanced device processes.
- An easy to specify product that will perform well across your entire range of device technologies.
- The opportunity to improve your total cost of ownership through elimination of furnace steps early in the fab process, when combined with MDZ®.
- Lower price and lower Cost of Ownership than competitive wafers.

Features	Benefits
Reduced COPs -> High GOI	Decreased possibility of yield and reliability degradation due to crystal related defects
Cost-effective manufacturing process	Cost-effective starting material alternative compared to other advanced wafers
Comparable performance with annealed wafers at much better cost	Lower Cost of Ownership than annealed wafers
Deep precipitate-free zone maintained throughout customer processing	Improved device yield and reliability potential by eliminating all oxygen precipitates in device layer
Robust IG protection through MDZ® which is consistent wafer to wafer and independent of initial oxygen	Insurance against device yield upsets caused by metallic contamination
Built-in IG template through MDZ® eliminates need for customer oxygen out-diffusion and nucleation	Improved customer cost of ownership through cycle time reduction

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10/04